IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Behrens et al.
Serial No.:	10/032,513
For:	DATA FLOW SYNCHRONIZATION
Filed:	26 OCT 2001
Examiner:	Juan A. Torres
Art Unit:	2611
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Attorney Docket Nos.: 20 01 0631
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants are submitting the present document concurrently with a notice of appeal for the above-noted application. Applicants are requesting that the Office review the final rejection of the claims as set forth in a final office action dated 28 SEP 2006. No amendments are being filed with this request.

Status of the Claims

Claims 1 - 11 are pending in the application, and stand finally rejected.

Clear Errors in the Examiner's Rejection

On page 8 of the Office Action, claims 1 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,324,664 to Farwell et al. (hereinafter "the Farwell et al. patent") in view of U.S. Patent No. 6,055,285 to Alston (hereinafter "the Alston patent").

Claim 1 provides for a testing unit for testing a device under test (DUT). The testing unit includes, *inter alia*, a synchronizing unit that receives a first clock signal from the DUT and a second clock signal from the testing unit. The synchronizing unit includes (a) a buffer for buffering data, (b) a write unit for writing data from the DUT into the buffer, wherein the first clock signal controls a write access onto the buffer, and (c) a read unit for reading out data from the buffer to be provided to a receiving unit, wherein the second clock signal controls a read access onto the buffer.

The Farwell et al. patent, with reference to FIG. 1, discloses an integrated circuit 10 coupled to external test equipment 33 via a test bus 31. Integrated circuit 10 includes combinatorial logic 15, a scan path 20, an output memory 25, a modulo counter 27, a read/write controller 19, and a test bus controller 29. A system clock (SYSCLK) clocks modulo counter 27 and scan path 20 (see FIG. 1), and test bus controller 29 provides a TEST CLOCK to read/write controller 19 (col. 4, lines 6 - 8). Read/write controller 19 (i) evaluates an index provided by modulo counter 27 to enable output memory 25 to sample the output of scan path 20, i.e., to write data into output memory 25, and (ii) in cooperation with test bus controller 29[1] reads output memory 25 (col. 3, line 65 - col. 4, line 8; and col. 4, lines 25 – 45). The Farwell et al. patent, at col. 5, lines 33 - 38, states:

> A scan test circuit has been described that employs a continuous system clock (SYSCLK) and accommodates a test clock (TEST CLOCK) that can be discontinuous or asynchronous relative to the system clock, and advantageously provides for scan testing of an integrated circuit that employs dynamic logic. (Emphasis added)

[1] The Farwell et al. patent, at col. 4, line 44, refers to "test bus controller 27", but from FIG.1, it is clear that the Farwell et al. patent intended to refer to "test bus controller 29."

The Alston patent is directed toward a synchronization circuit for transferring data between two asynchronous circuits (Abstract).

The Office Action, near the bottom of page 8, recognizes that the Farwell et al. patent does not specifically disclose that a first clock signal controls a write access into a buffer, and a second clock signal controls a read access onto the buffer. Therefore, the Office Action, on page 9, introduces the Alston patent, and states that it would have been obvious to supplement the apparatus disclosed by the Farwell et al. patent with the synchronization circuit disclosed by the Alston patent. The Office Action further indicates that the suggestion/motivation for combining the Farwell et al. and Alston patents would have been to synchronize the transfer of data. Applicants respectfully disagree with the Examiner's assessment of the Farwell et al. and Alston patents.

However, whereas the Farwell et al. patent expressly states that the system accommodates asynchronous clocks, there is no apparent need to modify the Farwell et al. patent to include the synchronization circuit of the Alston patent. Moreover, if the Farwell et al. patent were modified to include the synchronization circuit of the Alston patent, such a modification would obviate the manner in which modulo counter 27 and test bus controller 29 coordinate the writing of data to, and reading of data from, output memory 25, thus changing the principle of operation of the Farwell et al. patent. Hence, the cited combination of the Farwell et al. and Alston patent is **improper for purposes of a section 103(a) rejection** of claim 1. Accordingly, Applicants submit that claim 1 is patentable over the cited combination of the Farwell et al. and Alston patents.

Claims 2 - 7 depend from claim 1. By virtue of this dependence, claims 2 - 7 are also patentable over the cited combination of the Farwell et al. and Alston patents.

Claim 8 includes a recital similar to that of claim 1, as presented above. Accordingly, claim 8, for reasoning similar to that provided in support of claim 1, is patentable over the cited combination of the Farwell et al. and Alston patents.

Claims 9 - 11 depend from claim 8. By virtue of this dependence, claims 9 - 11 are also patentable over the cited combination of the Farwell et al. and Alston patents.

In view of the foregoing, Applicants respectfully request that the Office withdraw the rejection of claims 1 - 11.

Respectfully submitted,

12/27/06

Date

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